DOCUMENT-IDENTIFIER: US 5761517 A

TITLE: System and method for reducing power consumption in high

frequency

clocked circuits

DEPR:

Further, if the power.sub.-- high signal remains active through another

predetermined sampling period, the control state machine sends appropriate

select signals to the pattern generator and a 0001 bit pattern is output such

that 0100 is loaded into the shift register, thereby reducing the system clock

frequency to 25% of the oscillator clock frequency, since the inverting

registers cause a 0001 to be ANDed with the oscillator clock signal. If

necessary, a level 0 state could be reached which would completely turn off the

system clock. That is, a 0000 bit pattern would be output and a 0101 presented $\,$

to the shift register by the pattern generator wherein a 0000 will be $\overline{\text{ANDed}}$

with the oscillator clock. Various state levels 0 through 4 present the

opportunity by the present invention to generate a control signal to a power

supply which in response may lower the power supply voltage.

CCOR:

713/322

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